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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,484	YUUKI ET AL.	
	Examiner	Art Unit	
	Lawrence B. Williams	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 13* is/are allowed.

6)☒ Claim(s) *1-5,12 and 13* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed 04 September 2007, with respect to the rejection(s) of claim(s) 1-8, 10, 12-13 under U.S.C. 102 and U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gaudet U.S. Patent 6,285,726 B1, d'Haene et al. US Patent 6,614,314 B2, and Cheah et al. US Patent 6,888,905 B1.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3, 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaudet (US Patent 6,285,726 B1).

(1) With regard to claim 3, Gaudet discloses in Fig. 5, a digital-control type clock data recovery circuit comprising: a phase comparator (114) comparing a phase of input data with a phase of a data recovery clock signal generated internally (recovered clock phase mux and interpolator, 106), outputting a DOWN signal to delay said data recovery clock signal when a rising edge of said input data is detected during a first term after said data recovery clock signal (col. 6, lines 41-43, 55-59, 64-65) and outputting an UP signal to set forward the phase of said

data recovery clock signal when a falling edge is detected during a second term before said data recovery clock signal (col. 6, lines 41-43, 55-59, 62-64); a counter (132) for effectuating said UP signal when said UP signal is repeatedly generated and effectuating said DOWN signal when said DOWN signal is repeatedly generated (col. 7, lines 36-41); and a clock phase generation unit (phase selector, 140, phase mux, 142, 142 of phase mux & interpolator, 106) generating said data recovery clock signal and shifting the phase of said data recovery clock signal (RXC, 118 (data recovery clock) shifted through phase mux & interpolator, 106 through div2, 120; col. 5, lines 54-67; Gaudet discloses the clock signal (recovered clock, RXC) phase is adjusted by selecting a different phase of the N available phases provided by a clock generation module) on the basis of the effectuated UP signal and the effectuated DOWN signal (pu/pd) output from said counter (132); and wherein said input data is taken in with a timing of said data recovery clock (col. 3, lines 46-49); Gaudet discloses the RXC (data recovery clock signal) used to control sampling of the data in a phase picker architecture which is which his invention utilizes (col. 5, lines 54-55).

(2) With regard to claim 5, Gaudet also discloses wherein said clock-phase generation unit (106) includes a phase variable delay circuit (222, 138, 136) for generating N clock signals with phases different from each other (144, ph1-ph6) on the basis of a reference clock signal (Fig. 6, 202), and selecting one of said N clock signals as said recovered clock signal in accordance with a phase selection signal (phase selector, 140), where N is a finite number, and a cyclic clock phase pointer (delay selector, 136) setting and changing said phase selection signal in accordance with the effectuated UP signal and the effectuated DOWN signal (up/dn).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheah et al. (US Patent 6,888,905 B1) in view of d'Haene et al. (US Patent 6,614,314 B2).

Cheah et al. discloses in Fig(s). 16A-D, a data recovery method for generating a recovered clock signal (recovered clock) from said input data (oversampled data signal, 52) on the basis of a timing of said recovered clock signal, wherein a position of an edge of said input data is compared with a position of an edge of said recovered clock signal, and said edge of said recovered clock signal is kept away from said edge of said input data if a gap between said edge of said recovered clock signal and said edge of said input data becomes smaller than a predetermined reference value (col. 6, lines 42-67). Cheah et al. teaches increasing the counter by a cycle to advance the data signal when the leading edge of the recovered clock signal is "too close" to the falling edge of the data signal. A predetermined reference value signifying "too close" would be an inherent feature for proper operation of the timing recovery unit.

Cheah et al. does not disclose taking in said input data on the basis of a timing of said recovered clock signal.

However, d'Haene et al. discloses in Fig. 1, taking in input data on the basis of a timing of said recovered clock signal (col. 1, lines 37-42). d'Haene et al. teaches utilization of the

recovered clock signal to sample the input data signal in order to reduce or remove random phase deviations (jitter).

It would have been obvious to one skilled in the art at the time of invention to take in the input data on the basis of a recovered clock signal in order to reduce or remove random phase deviations (jitter) as disclosed by d'Haene et al.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheah et al. (US Patent 6,888,905 B1) in view of d'Haene et al. (US Patent 6,614,314 B2) as applied to claim 1 above, and further in view of Lee et al. (US 2002/0085656 A1).

As noted above, Cheah et al. in combination with d'Haene et al. disclose all limitations of claim 1 above. They do not disclose wherein a cycle of a reference clock signal is divided into N portions to generate N clock signals with phases different from each other, where N is a finite number, and one of said clock signals is selected as said recovered clock signal.

However, Lee et al. discloses in Fig. 4, a data recovery system wherein a cycle of a reference clock (402) signal is divided into N portions to generate N clock signals with phases different from each other, where N is a finite number (Fig. 4, pg. 3, paragraph 0030), and one of said clock signals is selected as said recovered clock signal (pg. 3, paragraph 0031; Lee et al. discloses the data sampler latching data on the triggering of the clock signals to provide recovered data. Thus the three phase clock signals act as recovered clock signals).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Lee et al. as a method of accurate phase tracking for a data link.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudet (US Patent 6,285,726 B1) as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art.

Claim 4 inherits all limitations of claim 3, above. As noted above, Gaudet discloses all limitations of claim 3. Gaudet does not disclose wherein the phase generating unit shifts the phase of said data recovery signal so as to separate an edge of said data recovery clock signal away from said rising and falling edge of said input data by a predetermined time gap.

However, Applicant's Admitted Prior Art teaches in Fig. 2, wherein the phase generating unit shifts the phase of said data recovery signal so as to separate an edge of said data recovery clock signal away from said rising and falling edge of said input data by a predetermined time gap (T/N).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of the prior art as a known method of reducing phase deviations (jitter).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over d'Haene et al. (US Patent 6,614,314 B2) in view of Cheah et al. (US Patent 6,888,905 B1).

d'Haene et al. discloses in Fig(s). 1, 2, 3a, a digital-control type clock data recovery circuit comprising: a control circuit (10) for comparing a position of an edge of data (22) with a position of an edge of a data recovery clock signal (20) in an eye (Fig. 3a) narrowed by high-frequency phase deviations (jitter) of said data, wherein said data is taken in with a timing of said edge of said data recovery clock signal (col. 1, lines 37-42), and wherein said control circuit

executes said control for placing said data recovery clock signal in an eye narrowed by high-frequency phase deviations (jitter) (col. col. 1, lines 27-50, col. 2, lines 55-59).

d'Haene et al. does not disclose execution of control to prevent a distance between said position of said edge of said data recovery clock signal and said position of said edge of data from becoming smaller than a predetermined value.

However, Cheah et al. teaches execution of control to prevent a distance between a position of an edge of said data recovery clock signal and a position of an edge of data from becoming smaller than a predetermined value (col. 6, lines 42-67). Cheah et al. teaches increasing the counter by a cycle to advance the data signal when the leading edge of the recovered clock signal is "too close" to the falling edge of the data signal. A predetermined value signifying "too close" would be an inherent feature for proper operation of the timing recovery unit.

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Cheah et al. to prevent misalignment of the leading edge of the clock signal and midpoint of the data signal to prevent transmission errors.

Allowable Subject Matter

9. Claims 10, 13 are allowed.

10. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a digital-control type clock data recovery circuit. A search of prior art references has failed to teach or suggest, a digital-control type clock data recovery circuit:

"wherein said function to track a wander of input data by comparing a position of an edge of said input data with a position of an edge of a clock signal is executed under a condition expressed by a relation given as follows: $B \times \sin(2\Pi \times Ta/Tw) < T/N$ where symbol B denotes a maximum phase change of said input data over a long period of time, symbol Ta denotes a loop delay, which is a period of time between an output operation carried out by a counter and a first phase comparison, symbol Tw denotes a phase deviation period, symbol T denotes a clock period, symbol N denotes the number of phase divisions, and T/N denotes a difference between 2 adjacent phases determined by said number of phase divisions N" as disclosed in claim 10.

" wherein said control circuit compares said position of said edge of said data recovery clock signal with said position of said edge of said data at a first predetermined frequency and changes a phase of said data clock recover signal at a second predetermined frequency not exceeding said first predetermined frequency", as disclosed in claim 13.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Hall discloses in US Patent 4,808,884 High Order Digital Phase-Locked Loop System, monitoring the occurrences of transition pulses to determine whether or not they occur in an up, central or down region.

b.) Ibukuro et al. discloses in US 2003/0215043 A1 PLO Device, sampling input data with a recovered clock signal.

c.) Shirota et al. discloses in US Patent 7,120,216 B2 Data/Clock Recovery Circuit For Recovering Data and Clock Signal With High Accuracy.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
November 11, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER